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				Application Number	10/627843
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				First Named Inventor	Ge Nong
				Art Unit	2824
				Examiner Name	Not Yet Assigned
Sheet	1	of	1	Attorney Docket Number	02-HK-076

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number Number-Kind Code <sup>2</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS					
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NON PATENT LITERATURE DOCUMENTS					
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PL	C1	Iyer, et al., "Analysis of a Memory Architecture for Fast Packet Buffers", In Proc. IEEE HPSR, Dallas, Texas, pp. 368-373; 2001, 7803-6711-1/01.			
PL	C2	Mike Clendenin; "IBM shows faster approach to embedded DRAM", EE Times, June 10, 2002. URL: <a href="http://www.embedded.com/showArticle.jhtml?articleID=10804520">http://www.embedded.com/showArticle.jhtml?articleID=10804520</a> .			

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